ADDITIONAL FEES:

No additional fees are believed required; however, should it be determined that a fee is due, authorization is hereby given to charge any such fee to our Deposit Account No. 01-0268.

REMARKS

In the Advisory Action mailed on March 18, 2003, the Examiner maintained the anticipatory rejection of claims 1 and 10-18 on the ground that the Figs. 22 and 5C structure of the cited reference to Nakamura discloses the claimed structure. The Examiner stated that the claims do not require a U-shaped surround structure.

By the present amendment, the specification and claims 1 and 10 have been amended to recite the U-shaped structure of the invention.

Applicant respectfully submits that claims 1 and 10-18 patentably distinguish over the prior art of record.

The present invention relates to an improved vertical MOS transistor structure. As set forth by amended independent claim 1 and independent claim 10, the inventive vertical MOS transistor has a first conductivity type semiconductor substrate, a first conductivity type epitaxial layer formed on the substrate, a second conductivity type body region formed on the epitaxial layer, a trench formed through

the body region to extend into the epitaxial layer, a gate insulator formed in the gate and having a U-shaped void, and a gate formed in the trench.

As further recited by independent claims 1 and 10, the gate is comprised of a gate insulating film formed in the trench, a polycrystalline silicon gate (claim 1) or a first gate material (claim 10) partially filling the trench and having a U-shaped void, and a second gate material formed in the U-shaped void so that the second gate material is surrounded by the first gate material (or polycrystalline silicon gate) and the gate insulator.

Claim 1 further recites that the second gate material is one of silicon oxide and silicon nitride.

Accordingly, the inventive vertical MOS transistor recited by independent claims 1 and 10 has a trench formed through a second conductivity body region and an epitaxial layer having the first conductivity type formed directly on a first conductivity type substrate. An insulating material having a U-shaped form is disposed in the trench. The gate fills the trench and is formed of a first gate material having a U-shaped form and a second gate material of polycrystalline silicon (claim 1) or an insulating material (claim 10) such as one of silicon oxide and silicon nitride (claim 1).

The claimed invention is disclosed, for example, in the embodiment illustrated in Fig. 11 of the application drawings. The vertical MOS transistor includes a first conductivity type semiconductor substrate 1, a first conductivity type epitaxial layer 2 formed on the substrate 1, and a second conductivity type body region 3 formed on the epitaxial layer 2. A U-shaped trench 4 is formed through the body region 3 to extend into the epitaxial layer 2. A gate oxide film 5 having a U-shaped form is formed on the side wall and bottom wall of the trench 4. A polysilicon gate 6 partially fills the trench so as to be surrounded by the gate oxide film 5. A silicon nitride or silicon oxide film 12 fills the portion of the trench not filled by the polysilicon gate 6 so as to be surrounded by the gate oxide film 5 and the polysilicon gate 6. A gate electrode 9a is connected to the polysilicon gate material. A source region 7 is formed in the body region 3 to surround the trench 4. A source electrode 7a is connected to the source region 7 and a drain electrode 1a is connected to the substrate 1.

Anticipation requires the disclosure, by a single reference, of all claimed subject matter. In the absence of any disclosure of a second gate material surrounded by a polycrystalline gate as required by each of independent claims 1 and 10, anticipation cannot be found. See, e.g., W.L. Gore

& Associates v. Garlock, Inc., 220 USPQ 303, 313 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984) ("Anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration"); Continental Can Co. USA v. Monsanto Co., 20 USPQ2d 1746, 1748 (Fed. Cir. 1991) ("When more than one reference is required to establish unpatentability of the claimed invention anticipation under § 102 can not be found"); and Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 221 USPQ 481, 485 (Fed. Cir. 1984) (emphasis added) ("Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim").

The polysilicon gate 22 of Nakamura does not have a U-shaped form. In addition, the oxide film 11 of Nakamura does not have a U-shaped form and is not surrounded by the polysilicon gate 22.

Accordingly, applicant respectfully submits that claims 1 and 10-18 are not anticipated by Nakamura and that the rejection under 35 U.S.C. §102(e) should be withdrawn.

In view of the foregoing amendments and discussion, the application is now believed to be in condition for

allowance. Accordingly, favorable reconsideration and allowance of the claims are most respectfully requested.

Respectfully submitted,

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MAILING CERTIFICATE

I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: COMMISSIONER OF PATENTS & TRADEMARKS, Washington, D.C. 20231, on the date indicated below.

Bruce L. Adams
Name

_____
Signature

March 28, 2003
Date

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Paragraph beginning 4 lines from the bottom of page 8 has been amended as follows:

--Fig. 1 is a sectional view of an N channel vertical MOS transistor according to the present invention. A semiconductor substrate is prepared in which a lightly doped layer 2 of a first conductive type is epitaxially grown on a heavily doped substrate 1 of the first conductive type to be a drain region. Then, a diffusion region 3 of a second conductive type referred to as a body region is formed from a surface of the semiconductor substrate by impurity implantation and high temperature thermal treatment at 1000°C or higher. Further, from the surface, a heavily doped impurity region 7 of the first conductive type to be a source region and a heavily doped body contact region 8 of the second conductive type for the purpose of fixing a potential of the body region by an ohmic contact are formed and are connected to a source electrode 7a and a body electrode 8a, respectively. Here, since a potential of the body contact region of the second conductive type and the potential of the body contact region of the second conductive type are the same, they are laid out so as to be in contact with each other

in Fig. 1. The source electrode 7a and the body electrode 8a are connected with each other through a contact hole, not shown in the figure, for electrically contacting the two regions. These are structured in the same way as those of the conventional transistor. Then, a trench 4 is formed by etching single crystalline silicon through the source region of the first conductive type. A gate insulating film 5 is formed in a U-shaped form on an inner wall of the silicon trench such that the gate insulating film 5 covers a side wall and a bottom surface of the trench and has an internal U-shaped void therein. Polycrystalline silicon 6 containing a high concentration of impurity is filled in a U-shaped form inside the internal void of the gate insulating film in the trench so that the polycrystalline silicon 6 itself has an internal U-shaped void with a sidewall and a bottom surface. Further, metal silicide 9 is formed inside the internal void of the polycrystalline silicon 6 film in the trench so as to be in contact with the polycrystalline silicon 6 along the direction of the trench. The polycrystalline silicon 6 containing a high concentration of impurity and the metal silicide 9 are connected to a gate electrode 9a. The heavily doped region of the first conductive type on a rear side of the semiconductor substrate is connected to a drain electrode 1a.--

IN THE CLAIMS:

Claims 1 and 10 have been amended as follows:

1. (Three Times Amended) A vertical MOS transistor comprising:

a semiconductor substrate having a first conductivity type;

an epitaxial growth layer having the first conductivity type formed on the semiconductor substrate;

a body region having a second conductivity type formed on the epitaxial growth layer;

a trench having a sidewall extending [formed] through the body region of the second conductivity type and having a bottom surface disposed [so as to reach] inside of the epitaxial growth layer of the first conductivity type;

a gate insulating film formed along an upper surface of the body region of the second conductivity type and the sidewall and the [a wall surface and a] bottom surface of the trench and having a U-shaped form so as to define a U-shaped void within the trench;

a polycrystalline silicon gate partially filling the internal void of the gate insulating film [trench so as to be in contact with the gate insulating film and surrounded by the gate insulating film];

a second gate material comprised of one of a silicon oxide film and a silicon nitride film filling a remaining portion of the internal void [trench] not filled by the polycrystalline silicon gate so as to be in contact with the polycrystalline silicon gate and having a sidewall and a bottom surface that are surrounded by the gate insulating film and the polycrystalline silicon gate;

a source region of the first conductivity type formed in the upper surface of the body region of the second conductivity type and around the trench so as to be in contact with the gate insulating film;

a gate electrode connected to the polycrystalline silicon gate and the second gate material;

a source electrode connected to the source region; and

a drain electrode connected to the semiconductor substrate.

10. (Amended) A vertical MOS transistor comprising: a semiconductor substrate having a first conductivity type; an epitaxial layer having the first conductivity type formed on the semiconductor substrate; a body region having a second conductivity type formed on the epitaxial layer; a trench extending through at least the body region and extending into the epitaxial layer; a gate insulator formed in the trench and

having a sidewall and a bottom surface defining a first U-shaped void; and a gate formed of a first gate material disposed in the U-shaped void of the gate insulator so that the first gate material has a second U-shaped void, [trench so as to be surrounded by the gate insulator] and a second gate material comprised of an insulating material disposed in the second U-shaped void [trench] so as to be surrounded by the gate insulator and the first gate material.